REMARKS

The present application was filed on October 9, 2001 with claims 1 through 30. Claims 1 through 30 are presently pending in the above-identified patent application. Claims 1, 10, 19, and 25 are proposed to be amended herein.

In the Office Action, the Examiner rejected claims 1, 10, 19, and 25 under 35 U.S.C. §102(a and/or b) as being anticipated by the admitted prior art in co-pending related patent application serial number 09/975,764 and rejected claims 2-9, 11-18, 20-24, and 26-30 under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in co-pending related patent application serial number 09/975,764.

The present invention is directed to a method and apparatus for allocating a section of a cache memory to one or more tasks. A set index value that identifies a corresponding set in the cache memory is transformed to a mapped set index value that constrains a given task to the corresponding allocated section of the cache. The allocated cache section of the cache can be varied by selecting an appropriate map function. When the map function is embodied as a logical and function, for example, individual sets can be included in an allocated section, for example, by setting a corresponding bit value to binary value of one. A cache addressing scheme is also disclosed that permits a desired portion of a cache to be selectively allocated to one or more tasks. A desired location and size of the allocated section of sets of the cache memory may be specified.

The specification has been amended to correct typographical errors.

Independent Claims 1, 10, 19 and 25

Independent claims 1, 10, 19, and 25 were rejected under 35 U.S.C. §102(a and/or b) as being anticipated by the admitted prior art in co-pending related patent application number 09/975,764. In particular, the Examiner asserts that the admitted prior art teaches "the frames/blocks in a set are allocated to a specific task while other frames/blocks in a different set are allocated to a different task."

Applicant notes that the admitted prior art is directed to methods and apparatus for adaptively locking and unlocking frames in such cache memories. The admitted prior art does not address the issue of restricting the access of secondary tasks, such that the secondary tasks may use *only* said allocated sets of said cache memory.

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independent claims 1, 10, 19, and 25, as amended, require wherein one or more secondary tasks may use *only* said allocated sets of said cache memory.

Thus, the admitted prior art does not disclose or suggest "wherein one or more secondary tasks may use only said allocated sets of said cache memory," as required by independent claims 1, 10, 19, and 25, as amended.

Dependent Claims 2-9, 11-18, 20-24 and 26-30

Dependent 2-9, 11-18, 20-24 and 26-30 claims were rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in co-pending related patent application number 09/975,764.

Claims 2-9, 11-18, 20-24 and 26-30 are dependent on claims 1, 10, 19, and 25, respectively, and are therefore patentably distinguished over the admitted prior art in co-pending related patent application serial number 09/975,764 because of their dependency from amended independent claims 1, 10, 19, and 25 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., Claims 1-30, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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